REMARKS

Entry of this amendment and reconsideration and allowance of this application, as amended, are respectfully requested.

The prior art grounds of rejection are respectfully traversed. In addition to our remarks made in prior submissions to the USPTO Applicant adds the following.

In Parulaki et al. (Pat. '406 & Pat. '607) and Whipple et al. (Pat. '215), thinning-out of lines is made with fast dump gate structure. In this technique, image signal of lines as the subject of the thinning-out (i.e., unnecessary lines) is swept off with a fast dump gate structure provided on vertical and horizontal transfer routes without being transferred to these routes. According to our claimed inventions, charge transfer from the site to the vertical transfer route is selected in units of lines in dependence on the operation mode, that is, it is attained without provision of any fast dump gate structure but with sole control of the read out signal.

According to Udagawa et al. (Pat. '781), the color filter array is not of the RCB array color system but of the (CMY + G) complementary system. The array is a cycle structure array different from that of the Bayer type. Pixel addition is strongly dependent on the color cycle structure of the color filter array, and therefore this color filter can not be easily combined with other techniques.

Our claimed inventions at least in part concern the read-out of color image signal from an area imager with Bayer type (primary color system) filter, and it features the provision of a mode for reading out image signal, which pertains to the sum of two or more integral number same color lines per three or more integral number lines in at least partly continuous six or more integral number lines (for AF), a mode for reading out image signal, which pertains to the sum of two or more integral number same color lines in three or more integral number

lines in the entire image frame area for AE and AWB, and a mode for reading out the entire pixels in the entire image frame area (for still image recording). With this structure, it is possible to sufficiently protect AE, AWB and AF sample plates of even an imager having a large number of pixels without raising the drive frequency.

In view of the above, a Notice of Allowance for the claims, as amended, is respectfully requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached Appendix is captioned **"Version with markings to show changes made"**.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,
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Enclosures: Appendix showing claim changes

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please amend the claims as follows:

14. (Amended) An electronic imaging system comprising:

a solid-state image sensor having a two-dimensional array of pixels capable of converting light incident thereon to electric signal, the pixels being arranged in a plurality of horizontal lines, the lines being arranged vertically one under another;

a color filter arranged on [a] an incident plane of the solid-state image sensor having a line sequential primary color mosaic pattern; and

control means for selectively controlling a mode for sequential scan reading out pixel signals concerning the whole pixels of the solid-state image sensor for still picture recording, and a mode for reading out pixel signal sums by utilizing a plurality of vertical registers each of n ($n \geq 2$, n being an integer) lines among m ($m \geq 3$, m being an integer) lines in k ($k \geq 6$, k being an integer) continuous lines of the solid-state image sensor for still picture recording or dynamic image processing.

15. (Amended) An electronic imaging system comprising:

a solid-state image sensor having a two-dimensional array of pixels capable of converting light incident thereon to electric signal, the pixels being arranged in a plurality of horizontal lines, the lines being arranged vertically one under another ;

a color filter arranged on [a] an incident plane of the solid-state image sensor having a line sequential primary color mosaic pattern ; and

control means for selectively controlling a mode for sequential scan reading out pixel signals concerning the whole pixels of the solid-state image sensor for still picture recording, a mode for reading out pixel signal sums by utilizing a plurality of vertical registers each of n ($n \geq 2$, n being an integer) lines among m ($m \geq 3$, m being an integer) lines of the solid-state image sensor for still picture recording or dynamic image processing, and a mode for reading out pixel signal sums by utilizing a plurality of vertical registers of n lines among m lines in k ($k \geq 6$, k being an integer) partially continuous lines of the solid-state image sensor for still picture recording or dynamic image processing.

38. (Amended) An electronic imaging system comprising:

a solid-state image sensor having a two-dimensional array of pixels capable of converting light incident thereon to electrical signals, the pixels being arranged in a plurality of horizontal lines, the lines being arranged vertically one under another ;

a color filter arranged on a incident plane of the solid-state image sensor having a line sequential primary color mosaic pattern; and

control means for selectively controlling a mode for sequential scan reading out pixel signal concerning the whole pixels of the solid-state image sensor for still picture recording and a mode for reading out pixel signal sums of n lines out of every m lines within partially continuous k lines of the solid-state image sensor by utilizing a plurality or vertical registers for still picture recording or dynamic image processing, wherein

$n \geq 2$, n being an even number,

$m \geq n+1$, m being an odd number,

$k \geq 2m$, k being an integer.